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B-2750 FWC / 615179-4

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: SAU-GEE CHEN and CHIEH-CHIH LI

Serial No.: 08/510,740

Filed: August 2, 1995

Title: METHOD FOR FINDING QUOTIENT IN A DIGITAL SYSTEM

Examiner: E. Moise

Art Unit: 2306

Re: APPELLANT'S BRIEF

Our Ref.: B-2750 FWC 615179-4

Date: June 2, 1997

I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on:

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Richard J. Paciulan
Name of Person Signing

Richard J. Paciulan
Signature

REPLY BRIEF

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

The present application is under appeal to the Board of Patent Appeals and Interferences, the Notice of Appeal having been mailed on October 21, 1996, and the Appeal Brief having been mailed on December 20, 1997. This Reply Brief is in response to the Examiner's Answer, dated April 1, 1997.

A. NEW POINTS OF ARGUMENT RAISED IN THE EXAMINER'S ANSWER

1. Grouping of Claims

The Examiner states in the Examiner's Answer that the rejection of claims 1-4 stands or falls together because Appellant's brief does not include a statement that this grouping of claims does not stand or fall together. This is a point of argument raised by the Examiner for the first time in the Examiner's Answer. Therefore, pursuant to 37 CFR 1.193, the Appellant may properly present rebuttal argument against this new point of argument raised by the Examiner.

2. Response to Appellant's Argument

The Examiner states in the Examiner's Answer that the claims in the present application are not written in means-plus-function format, and that the claims do not recite a general purpose computer programmed to perform the claimed calculations. Therefore, the Examiner concludes that In re Alappat, 31 USPQ 2d 1545 (1994) is not controlling "since [claims 1-4] are not written in means-plus functions that represent specific digital circuitry structure."

The Examiner goes on to state that Claims 1-4 of the present application are directed to the solution of a mathematical problem, and to the preemption of a mathematical algorithm. Therefore, the Examiner concludes that these claims are non-statutory under 35 U.S.C. §101.

These arguments presented by the Examiner are new to this appeal. Accordingly, under 37 CFR 1.193, the Appellant may properly present a rebuttal argument to the Examiner's arguments.

B. REPLY TO NEW POINTS OF ARGUMENT

1. Grouping of Claims

The Examiner states in the Examiner's Answer that the rejection of Claims 1-4 stands or falls together because Appellant's brief does not include a statement that this grouping of claims does not stand or fall together.

The Appellant respectfully submits that the Appellant's Appeal Brief contains a statement to the effect that the grouping of claims does not stand or fall together. Specifically, reference is made to Section E of the Answer, entitled "Grouping of the Claims". In this section, the Appellant states that "each one of the claims is separately patentable, and, if the ground of rejection is sustained as to any one of the rejected claims, it is submitted that such rejection will not be applicable to all of the claims. (Appeal Brief, page 9, line 22 to page 10, line 1). Later in this same section, the Appellant presents argument supporting this statement. It appears that the Examiner may have overlooked this section in reaching the conclusion that the statement (to the effect that the grouping of claims 1-4 does not stand or fall together) is not found in the Appeal Brief. The Appellant therefore submits that Section E of the Appeal Brief adequately complies with 37 CFR 1.192(7), requiring "a statement. . .that the claims of the group do not stand or fall together. . . ."

2. Response to Appellant's Arguments

In the Examiner's Answer, the Examiner argues that the claims in the present application are not written in means-plus-function format, and that the claims do not recite a general purpose computer programmed to perform the claimed calculations. Therefore, the Examiner asserts that the present application cannot be compared to that of Alappat "since [claims 1-4] are not written in means-plus functions that represent specific digital circuitry structure." Contrasting the claims of the present invention to those of Alappat,

the Examiner concludes that "claims 1-4 and the disclosure are directed to the solution of a mathematical problem . . . . [T]he claims are directed to the preemption of a mathematical algorithm, and are thus non statutory."

It is noted that the Examiner has not presented any argument against many points made by the Appellant in its Appeal Brief. It is presumed by the Appellant that such points are accepted by the Examiner as not being in dispute in this Appeal. Specifically, the following points were not disputed by the Examiner.

- Patentability is not precluded from inventions constituting the application of computer software to computer systems. (See Appellant's Brief, page 11, line 23 to page 12, line 1).

- The application of a scientific truth, law of nature, or a mathematical formula to an otherwise statutory structure or process is not precluded from patentability. (See Appellant's Brief, page 12, lines 25-27 and page 15, lines 9-12). More specifically, the application of a series of mathematical steps (an algorithm or program) to a general purpose computer is not precluded from patentability. (See Appellant's Brief, page 15, line 13 to page 16, line 23).

Rather than argue against these points, the Examiner attempts to limit the applicability of the Alappat decision. To accomplish this, the Examiner argues that Claims 1-4 of the present application (unlike Claim 15 of Alappat) are not written in means-plus-function terminology representing specific digital circuitry structure, thereby rendering Alappat inapplicable to the present application. (Examiner's Answer, page 5, lines 2-4).

It is the Appellant's position that the holding of Alappat is not limited to means-plus-function claims. In Alappat, the Court of Appeals for the Federal Circuit (CAFC) was presented with the issue of whether the appealed claims of Alappat were directed to a "machine", one of the categories of patentable subject matter named in 35 U.S.C. §101.

(Alappat at 1551). The CAFC therefore focused its analysis on the determination of patentability under 35 U.S.C. §101. Citing the Supreme Court's decision in Diamond v. Diehr, 450 U.S. 175, 185, 209 USPQ 1 (1981), the CAFC held that "the dispositive inquiry is whether the claim *as a whole* is directed to statutory subject matter". (Alappat at 1557, emphasis in original). As such, the CAFC concluded that "it is irrelevant that a claim may contain, as part of the whole, subject matter which would not be patentable by itself. 'A claim drawn to subject matter otherwise statutory does not become nonstatutory simply because it uses a mathematical formula, [mathematical equation, mathematical algorithm,] computer program or digital computer.'" (Alappat at 1557; citations and footnotes omitted; revision marks in original). The court never states or suggests, in this recitation of law or in its subsequent application, that these principles only apply to means-plus-function claims. Indeed, such a conclusion finds no basis in law or logic.

Limiting patent protection of a programmed computer only to means-plus-function claims would necessarily bar such patent protection for substantially the same claims placed in method form. In other words, a conclusion that Alappat is limited in applicability only to means-plus-function claims also necessarily limits this case's applicability to apparatus claims. However, as discussed above, the CAFC in Alappat concerned itself with the determination of patentability under 35 U.S.C. §101. This law does not distinguish between apparatus claims (which may contain means-plus-function language) and method claims (which may not). Therefore, the holding of Alappat cannot logically be limited only to means-plus-function claims, and it is the Appellant's position that the applicability of Alappat is irrespective of claim form.

The Examiner also argues that Claims 1-4 of the present application are not drawn to a general purpose computer programmed to perform the claimed calculations. We have argued above that Alappat is applicable to the claims of the present application. As such, the similarity between Claim 1 of the present application and Claim 15 of Alappat's application, along with the similarity between the subject matter of the claims in both

applications, leads to the conclusion that the claims of the present application are directed to statutory subject matter as required by 35 U.S.C. §101.

In Alappat, the CAFC was presented with a claim (Claim 15) calling for a rasterizer comprising four means elements. (Alappat at 1553). In making a determination whether Claim 15 was directed to statutory subject matter as required by 35 U.S.C. §101, the court looked to Alappat's specification to identify the structure supporting the means elements in Claim 15. (Alappat at 1555). Once the supporting structure was identified, the court made its patentability decision based on the supporting structure in the specification.

Claim 1 of the present invention calls for:

> In a system for digital information processing, said system having a memory, a method for generating data representative of a quotient $Q = a_0a_1a_2....a_b$ from data representative of a divisor $Y = y_1y_2....y_n$ and data representative of a dividend $X = x_1x_2....x_a$, comprising the steps of (a) aligning . . . (l) storing in said memory as said data representative of a quotient, a quotient resulting from step (k). (Emphasis added).

Claim 2 also calls for a method in a system (having a memory) for digital information processing. Claims 3 and 4 both call for a system for digital information processing having a memory.

Just as the CAFC in Alappat followed 35 U.S.C. §112, paragraph 6 in identifying the structure and elements in Alappat's specification corresponding to the means-plus-function elements in Claim 15, 37 CFR 1.75 directs the meaning of terms found in claims to be "ascertainable by reference to the description". A "digital information processing system" by its own terms means a digital system (such as a computer, electronic

processor, etc.) capable of processing information. Supporting definition for a "digital information processing system" is found on page 17, line 20 of the present application:

> . . .digital information processing system 10 includes arithmetic unit 12 and memory 14. Arithmetic unit 12 typically contains VLSI binary logic circuit elements (such as adders, shifters, exclusive-or circuits, etc.) which, under system control, receives binary divisor and dividend data from memory 14, performs the steps of the invention, and thereupon provides the resulting quotient data back to memory 14. Those skilled in the art of digital information processing systems can readily provide the interconnection of needed logic circuit elements (and their appropriate control) to implement the invention." (Emphasis added).

From this description, earlier reference to the invention as a "digital system" (page 1, line 10), Figure 1 (showing an arithmetic logic unit and memory), and from the very text of Claims 1-4, the present invention is clearly directed to the implementation of an algorithm on an digital information processing system having specific digital circuitry structure. Claims 3-4 recite a machine, or apparatus made up of a combination of known electronic circuitry elements, while Claims 1-2 recite a method for generating quotient data on such a machine or apparatus. Limited to the realm of digital information processing systems, Claims 1-4 are therefore not "as a whole . . . a disembodied mathematical concept . . . which in essence represents nothing more than a 'law of nature,' 'natural phenomenon,' or 'abstract idea.'" (Alappat at 1557, citing Diehr; emphasis in original).

Just the opposite of being "disembodied", the present invention is embodied in a concrete and defined digital information processing system. Furthermore, the present invention does more than merely "manipulat[e] an abstract idea or solv[e] a purely mathematical problem without any practical limitation." (Examiner's Answer, page 5). The present invention does not just recite an algorithm - it performs an algorithm and applies the algorithm to a digital information processing system to enable the system

hardware to run faster and more efficiently.

Alappat's Claim 15 was held by the CAFC to be worthy of patent protection. The Examiner of the present application has determined that Claims 1-4 are not worthy of patent protection. However, a comparison of Alappat's Claim 15 and Claims 1-4 of the present application reveals nothing to justify different patentability determinations. The preamble of Alappat's Claim 15 calls for a "rasterizer", while the preamble of the present invention recites a "system for digital information processing". It should be noted that the CAFC considered Alappat's preamble important to the determination of patentability under 35 U.S.C. §101: "the claim preamble's recitation that the subject matter for which Alappat seeks patent protection is a rasterizer for creating a smooth waveform is not a mere field-of-use label having no significance." (Alappat at 1558).

Claim 15 of Alappat as interpreted by the court in light of the specification calls for an arithmetic logic circuit. Claims 1-4 of the present invention interpreted in the same manner calls for an arithmetic logic unit or its equivalent. (See Figure 1 and page 17, line 20 of the present application). Claim 15 of Alappat as interpreted by the court in light of the specification calls for a read only memory (ROM). Claims 1-4 of the present invention specifically recite a memory. Apart from Alappat's use of means-plus-function terminology within Claim 15 (which we have already argued above is irrelevant for a patentability determination under 35 U.S.C. §101), no difference between Claim 15 of Alappat and Claims 1-4 of the present invention exists to justify a conclusion that Claim 15 of Alappat is patentable and Claims 1-4 of the present application are not.

Claims 1-4 of the present application are drawn to a machine or apparatus, or to a method on a machine or apparatus, implementing an algorithm to improve the speed with which the machine or apparatus calculates quotients. Such an improvement falls squarely within the patentable subject matter categories of 35 U.S.C. §101, and is exactly the kind of technology which the patent laws are designed to protect.

Claims 1-4 do not amount to the preemption of a mathematical algorithm. These claims cannot be read upon by mental steps or processes. Rather, as in Alappat, Claims 1-4 are clearly restricted to a digital information processing system, i.e., a computer. No preemption occurs by patenting this invention. Alappat and the Supreme Court cases which preceded it make it clear that a programmed computer is a new machine, and the Appellant submits that when a new machine performs a new method, both the machine and the method are subject matter the patent laws should properly protect.

C. CONCLUSION

The Appellant has shown above that each of the Examiner's rejections are unfounded. Therefore, the Board is requested to reverse: the rejection of Claims 1-4 under 35 USC 101.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account 12-0415 and, in particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

Respectfully submitted,
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